

A 0.5-nm-thick layer of Fe was deposited, then patterned into catalyst islands for initiating growth of carbon nanotubes by means of photolithography and liftoff. To grow the carbon nanotubes, the workpiece as processed thus far was then placed in a chemical-vapor-deposition furnace, wherein it was exposed to an atmosphere of flowing CH_4 and H_2 at a temperature of 850 °C for 10 minutes. Next, a layer of Au/Ti was deposited and patterned in a lift-off process to form the source and drain electrodes in contact with the ends of the nanotubes.

Tests have confirmed the expected advantages of these devices over the older

electrostatically actuated microelectromechanical switches, which are characterized by response times of $\approx 1 \mu\text{s}$ and switching potentials between 60 and 70 V. The present devices are not only smaller but are characterized by response times of a few nanoseconds and switching potentials of a few volts. Hence, the present devices are expected to be better suited for applications in which there are requirements for highly miniaturized, high-speed electronic switches that can be operated from low-voltage (e.g., battery) power sources.

This work was done by Anupama Kaul, Eric Wong, and Larry Epp of Caltech for NASA's Jet Propulsion Laboratory.

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-43343, volume and number of this NASA Tech Briefs issue, and the page number.

Solid-State High-Temperature Power Cells

These cells can be used in batteries for high-temperature applications.

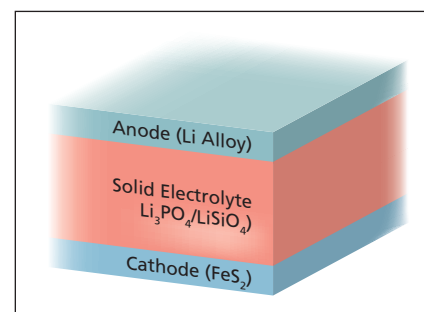
NASA's Jet Propulsion Laboratory, Pasadena, California

All-solid-state electrochemical power cells have been fabricated and tested in a continuing effort to develop batteries for instruments for use in environments as hot as 500 °C. Batteries of this type are needed for exploration of Venus, and could be used on Earth for such applications as measuring physical and chemical conditions in geothermal and oil wells, processing furnaces, and combustion engines.

In the state-of-the-art predecessors of the present solid-state power cells, fully packaged molten eutectic salts are used as electrolytes. The molten-salt-based cells can be susceptible to significant amounts of self-discharge and corrosion when used for extended times at elevated temperatures. In contrast, all-solid-state cells such as the present ones are expected to be capable of operating for many days at temperatures up to 500 °C, without significant self-discharge.

The solid-state cell described here includes a cathode made of FeS_2 , an electrolyte consisting of a crystalline solid solution of equimolar amounts of Li_3PO_4 and Li_4SiO_4 , and an anode made of an alloy of Li and Si (see figure). The starting material for making the solid electrolyte is a stoichiometric mixture of Li_3PO_4 , SiO_2 , and Li_2CO_3 . This mixture is ball-milled, then calcined for two hours at a temperature of 1,100 °C, then placed in a die atop the cathode material. Next, the layers in the die are squeezed together at a pressure between 60 and 120 MPa for one hour at a temperature of 600 °C to form a unitary structure comprising the solid electrolyte and cathode bonded together. Finally, the lithium-alloy anode is pressure-bonded to the solid electrolyte layer, using an intermediate layer of pure lithium.

In one test of a cell of this type, a discharge rate of about 1 mA per gram of cathode material was sustained for 72



This All-Solid-State Cell is capable of generating electric power at a temperature up to 500 °C.

hours at a temperature of about 460 °C. This is about three times the discharge rate required to support some of the longer duration Venus-exploration mission scenarios.

This work was done by Jay Whitacre and William West of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1), NPO-44396

Fast Offset Laser Phase-Locking System

Phases can be locked within a microcycle; known phase noise can be added.

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Figure 1 shows a simplified block diagram of an improved optoelectronic system for locking the phase of one laser to that of another laser with an adjustable offset frequency specified by the user. In comparison with prior systems, this system exhibits higher performance (in-

cluding higher stability) and is much easier to use. The system is based on a field-programmable gate array (FPGA) and operates almost entirely digitally; hence, it is easily adaptable to many different systems. The system achieves phase stability of less than a microcycle.

It was developed to satisfy the phase-stability requirement for a planned spaceborne gravitational-wave-detecting heterodyne laser interferometer (LISA). The system has potential terrestrial utility in communications, lidar, and other applications.

The present system includes a fast phasemeter that is a companion to the microcycle-accurate one described in “High-Accuracy, High-Dynamic-Range Phase-Measurement System” (NPO-41927), *NASA Tech Briefs*, Vol. 31, No. 6 (June 2007), page 22. In the present system (as in the previously reported one), beams from the two lasers (here denoted the master and slave lasers) interfere on a photodiode. The heterodyne photodiode output is digitized and fed to the fast phasemeter, which produces suitably conditioned, low-latency analog control signals which lock the phase of the slave laser to that of the master laser. These control signals are used to drive a thermal and a piezoelectric transducer that adjust the frequency and phase of the slave-laser output.

The output of the photodiode is a heterodyne signal at the difference between the frequencies of the two lasers. (The difference is currently required to be less than 20 MHz due to the Nyquist limit of the current sampling rate. We foresee few problems in doubling this limit using current equipment.) Within the phasemeter, the photodiode-output signal is digitized to 15 bits at a sampling frequency of 40 MHz by use of the same analog-to-digital converter (ADC) as that of the previously reported phasemeter. The ADC output is passed to the FPGA, wherein the signal is demodulated using a digitally generated oscillator signal at the offset locking frequency specified by the user. The demodulated signal is low-pass filtered, decimated to a sample rate of 1 MHz, then filtered again. The decimated and filtered signal is converted to an analog output by a 1 MHz, 16-bit digital-to-analog converters. After a simple low-pass filter, these analog signals drive the thermal and piezoelectric transducers of the laser.

Although the system phase-locks the two lasers to within a microcycle, in the original application, there is an occasional need to analyze the performance of the phasemeter in the presence of noise in the difference between the

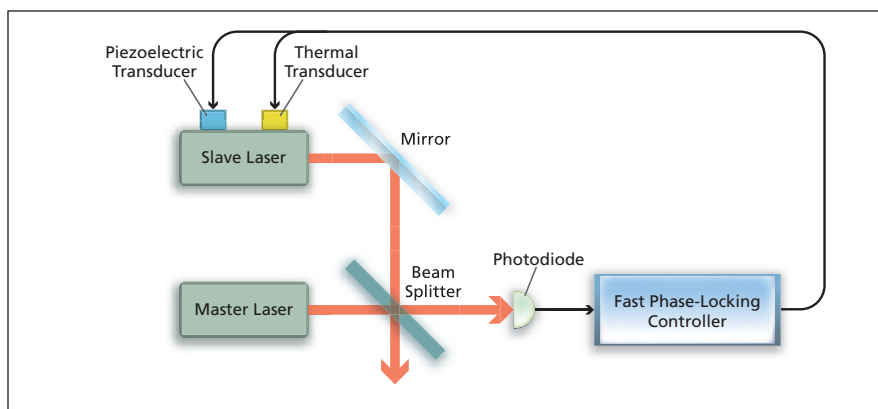


Figure 1. In the **Fast Offset Laser Phase-Locking System**, as in other such systems, a control signal is derived from the heterodyne signal arising from interference of two laser beams on a photodiode. The main innovative features of this system are embodied in the fast phase-locking controller, which is based on a mostly digital phasemeter.

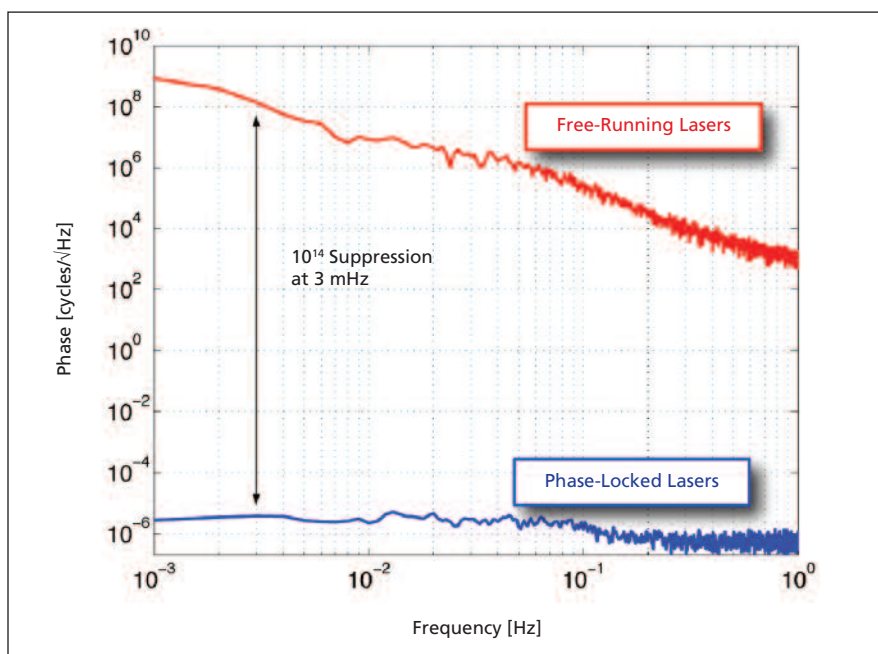


Figure 2. The **Performance of the Fast Offset Laser Phase-Locking System** is shown, as measured over the signal band, by the phasemeter described in NPO-41927.

phases and frequencies between the two lasers. This system includes a subsystem, based on a pseudorandom-number generator, that can add an adjustable amplitude phase noise characterized by a uniform, Gaussian, or $1/f$ distributions (where f denotes frequency). Figure 2 shows the per-

formance of the phase-locking system, and also noise added by the pseudorandom noise generator to mimic that of free-running lasers.

This work was done by Daniel Shaddock and Brent Ware of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44740